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Tsai et al.

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(54) **INTERCONNECTION STRUCTURE HAVING A VIA STRUCTURE**

(71) Applicant: **DELTA ELECTRONICS, INC.**, Taoyuan Hsien (TW)

(72) Inventors: **Hsin-Chang Tsai**, Taoyuan Hsien (TW); **Chia-Yen Lee**, Taoyuan Hsien (TW); **Peng-Hisn Lee**, Taoyuan Hsien (TW)

(73) Assignee: **DELTA ELECTRONICS, INC.**, Taoyuan (TW)

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CPC ***H01L 24/91*** (2013.01); ***H01L 21/76898*** (2013.01); ***H01L 23/481*** (2013.01); ***H01L 23/49562*** (2013.01); ***H01L 23/49575*** (2013.01); ***H01L 25/074*** (2013.01); ***H01L 25/18*** (2013.01); ***H01L 25/50*** (2013.01); *H01L 24/03* (2013.01); *H01L 24/05* (2013.01); *H01L 24/13* (2013.01); *H01L 24/16* (2013.01); *H01L 24/81* (2013.01); *H01L 2224/02372* (2013.01); *H01L 2224/0332* (2013.01); *H01L 2224/0401* (2013.01); *H01L 2224/05009* (2013.01); *H01L 2224/0557* (2013.01); *H01L 2224/05147* (2013.01); *H01L 2224/05548* (2013.01); *H01L 2224/06181* (2013.01); *H01L 2224/131* (2013.01); *H01L 2224/13024* (2013.01); *H01L 2224/13147* (2013.01); *H01L 2224/16146* (2013.01); *H01L 2224/16148* (2013.01); *H01L 2224/81193* (2013.01); *H01L 2224/81815* (2013.01);
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USPC 257/750, 774, 773, 737, 738, 784, 786, 257/734
See application file for complete search history.

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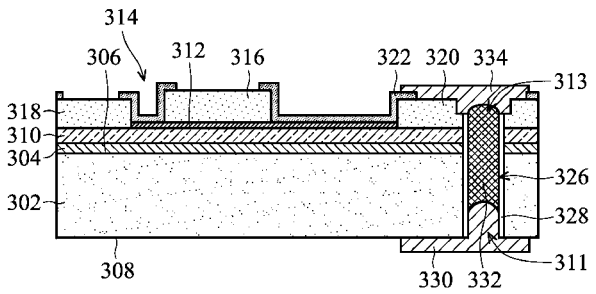
Primary Examiner — Alexander Oscar Williams
(74) *Attorney, Agent, or Firm* — Muncy, Geissler, Olds & Lowe, P.C.

(57) **ABSTRACT**

An interconnection structure is provided having a substrate with at least one electric device formed adjacent to a first side of the substrate and a via hole formed therethrough. The via hole has a first opening adjacent to the first side of the substrate. A via structure is disposed in the via hole without exceeding the first opening. A first pad is disposed on the first side of the substrate and covers the via hole. A second pad is disposed on a second side of the substrate opposite to the first side, wherein the via structure extends into the second pad. The first pad is adjoined to the via structure and electrically connects with the at least one electric device, and the first pad has a protrusion portion extending into the via hole.

18 Claims, 7 Drawing Sheets



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H01L 25/07	(2006.01)
H01L 25/18	(2006.01)
H01L 25/00	(2006.01)
H01L 23/495	(2006.01)

(52) **U.S. Cl.**

CPC *H01L2924/00014* (2013.01); *H01L 2924/13064* (2013.01)

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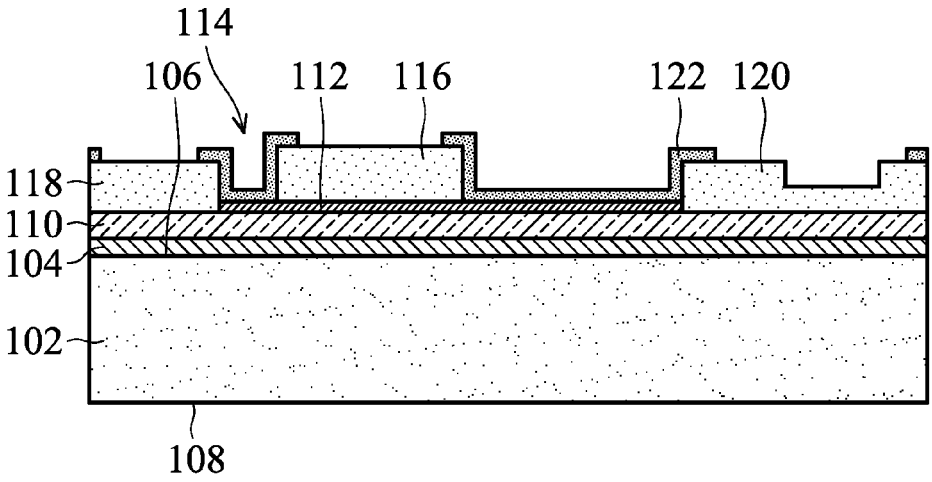
114
106
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102
108

FIG. 1A

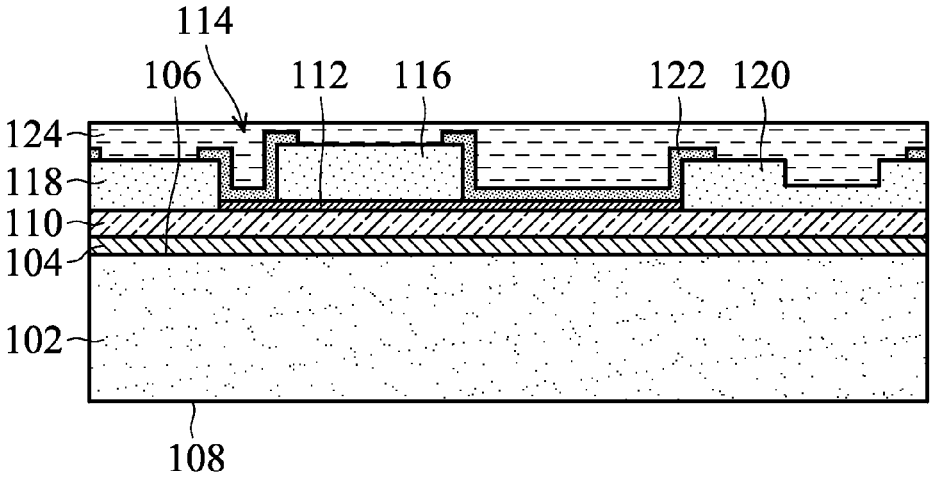
114
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FIG. 1B

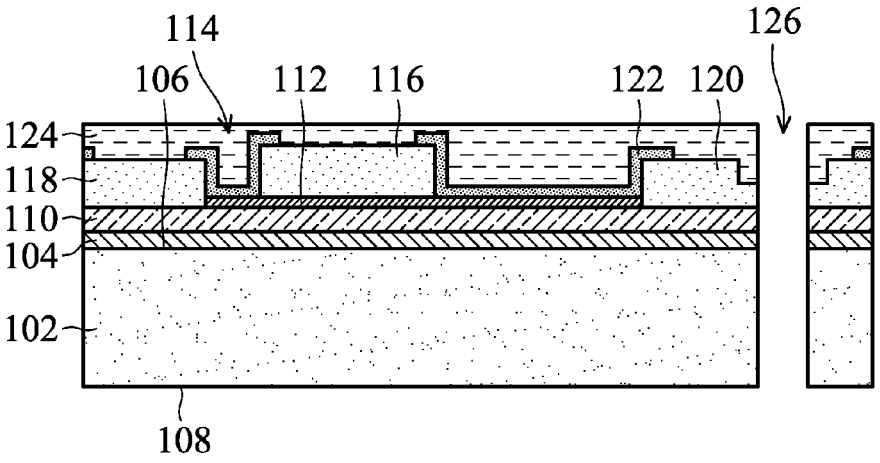
114
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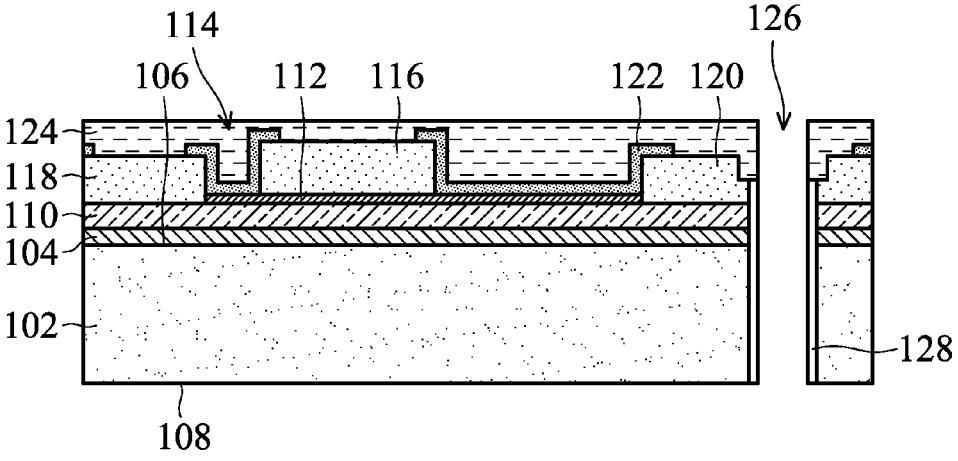
FIG. 1C


114
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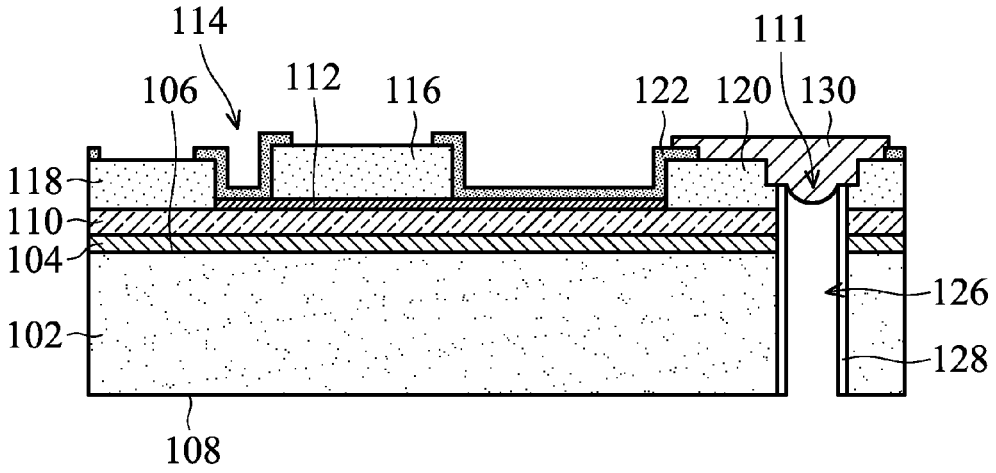
102
128
108

FIG. 1D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126
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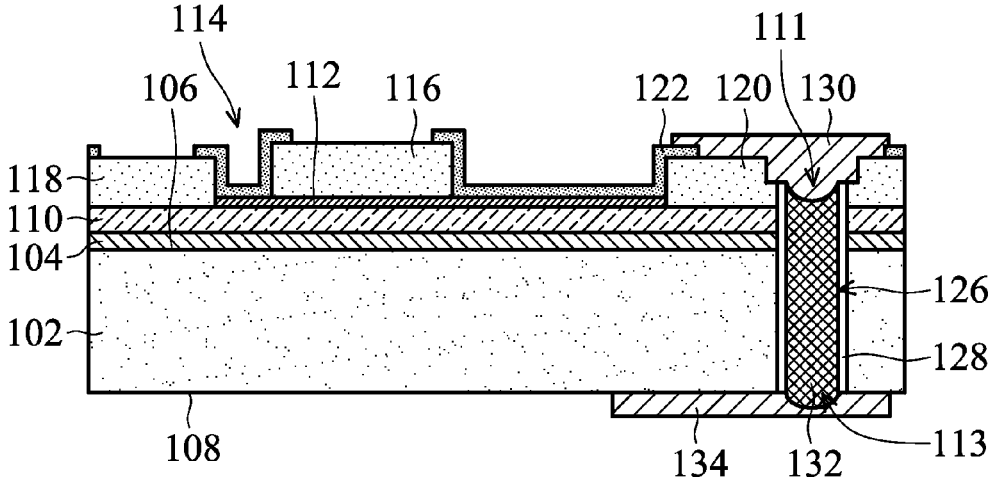
128
108

FIG. 1E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116
122
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130
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110
104
126
102
128
108
134
132
113

FIG. 1F

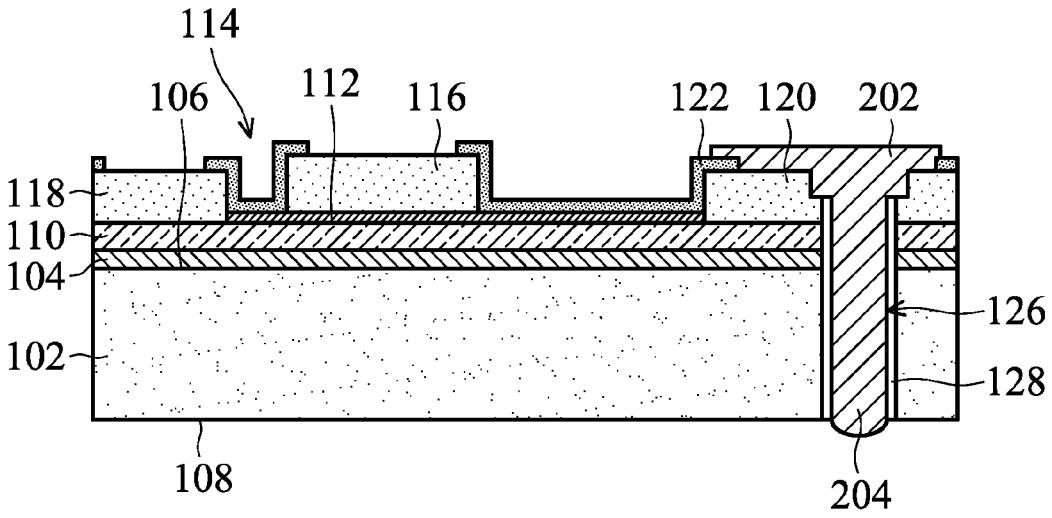
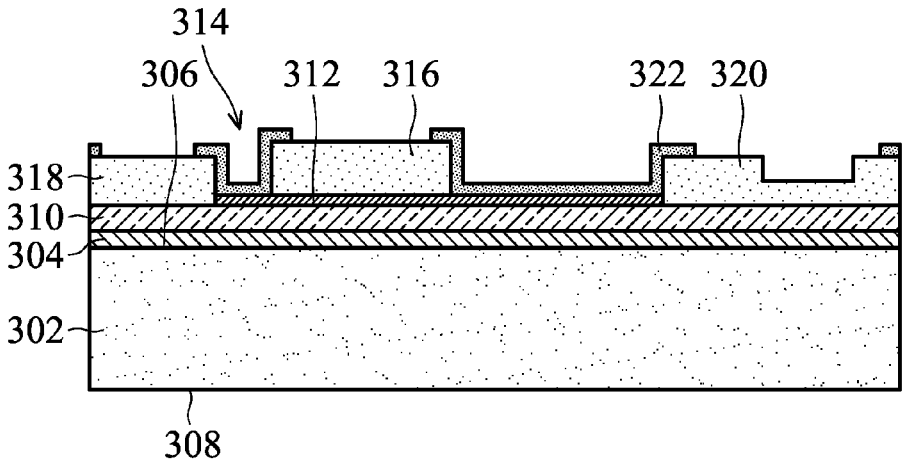


FIG. 2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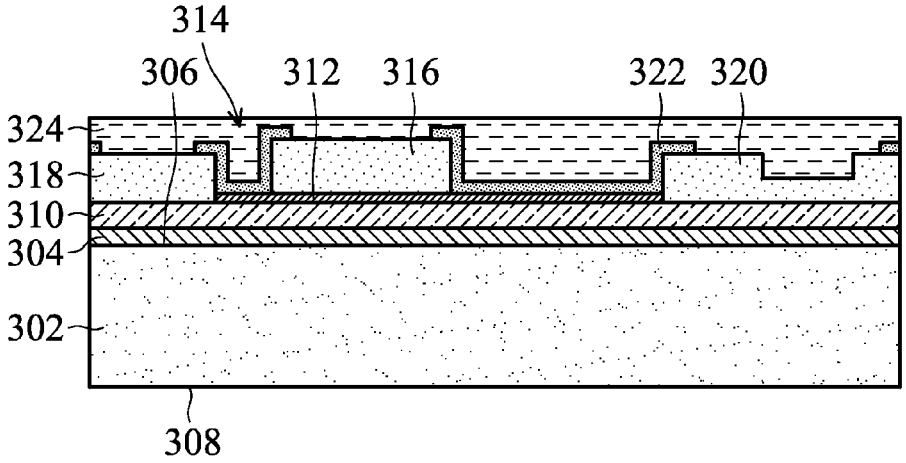
302
308

FIG. 3A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324
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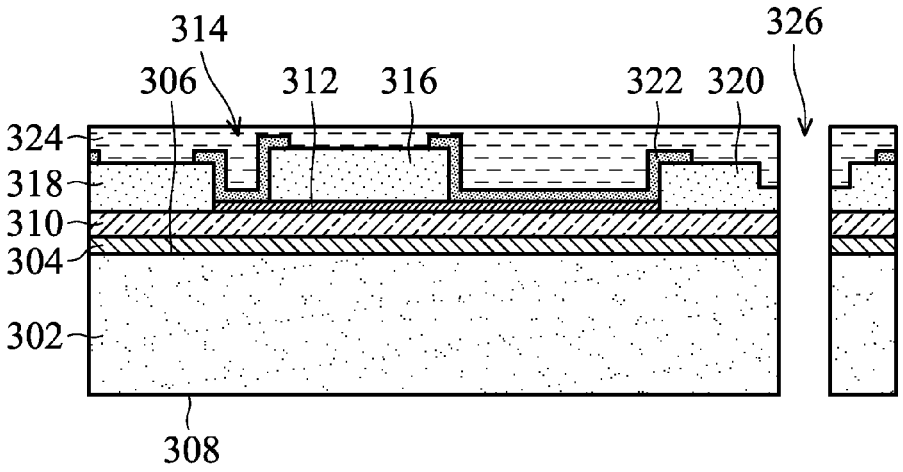
FIG. 3B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326
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324
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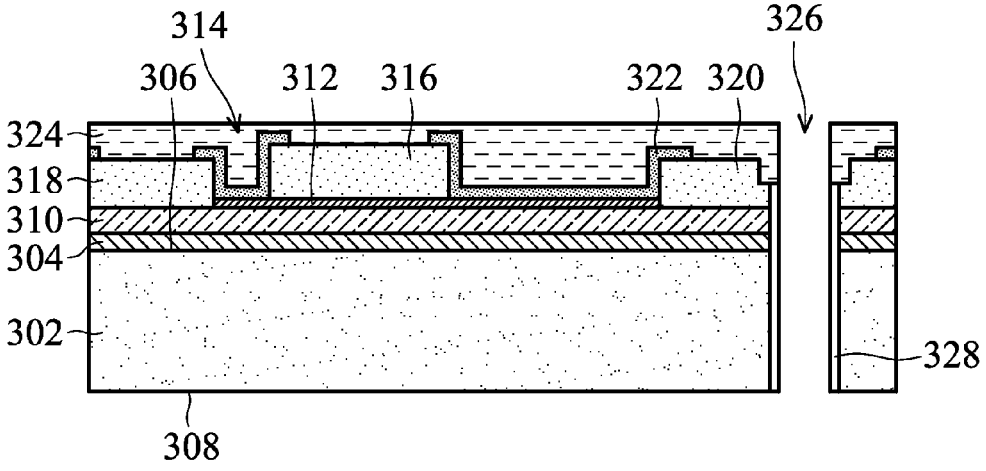
302
308

FIG. 3C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328
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FIG. 3D

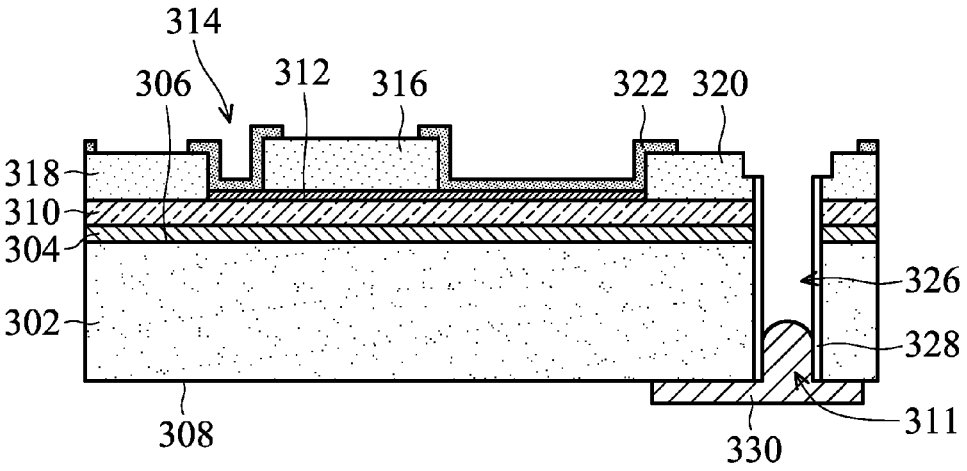
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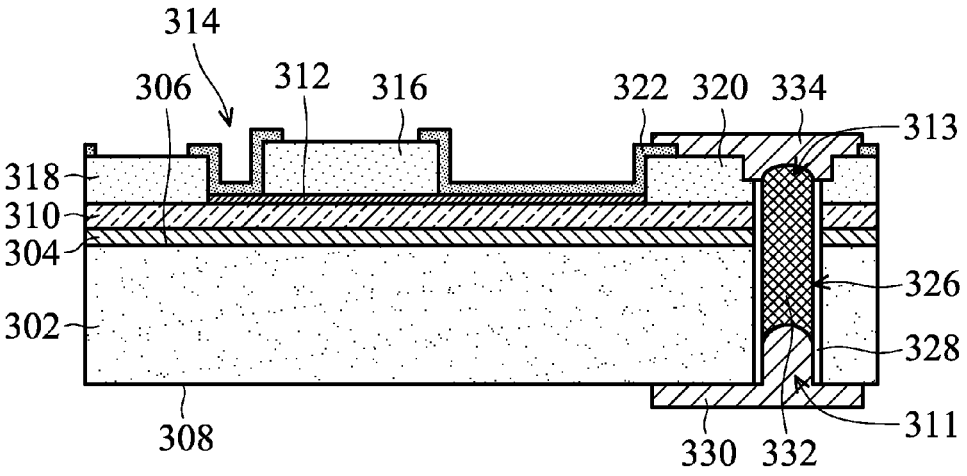
FIG. 3E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334
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318
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326
302
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311
330
332

FIG. 3F

INTERCONNECTION STRUCTURE HAVING A VIA STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to semiconductor manufacturing, and specifically, to a method for fabricating semiconductor components and interconnects with contacts on opposing sides.

2. Description of the Related Art

Semiconductor components include external contacts that allow electrical connections to be made from the outside to the integrated circuits contained in the semiconductor components. A semiconductor die, for example, includes patterns of bond pads formed on the face of the die. Semiconductor packages, such as chip scale packages, also include external contacts. Typically, a component includes only one set of external contacts on either the face side (circuit side) or the back side of the component. However, it is sometimes necessary for a component to have external contacts on both sides.

In semiconductor technology, a through-silicon via, also known as a through-substrate via, is a conductive feature formed in a semiconductor substrate (wafer or die) to electrically connect external contacts from both sides. The TSV feature vertically passes through the semiconductor substrate, providing for stacked wafer/die packaging methods and allowing for electrical connection between circuits within separate wafers or chips. There are a number of ways to create a TSV. Typically, a hole is etched into the semiconductor substrate, and sometimes through the interconnect structure as well. The hole may then be lined with various isolating layers and/or various metal layers. The hole is then filled with a conductive material, typically copper (Cu), which becomes the major part of a TSV.

In traditional technologies, an electrode electroplating method is used for the conducive filling materials to be disposed in the hole of the through silicon via (TSV), wherein a seeding layer is formed by a vacuum technique, such as plasma vapor deposition, prior to formation of the conductive filling material. The vacuum technique requires high priced equipment, which increases device costs.

BRIEF SUMMARY OF INVENTION

The invention provides an interconnection structure. A substrate has at least one electric device formed adjacent to a first side of the substrate and a via hole formed therethrough. A via structure is disposed in the via hole having a first side neighboring the first side of the substrate, wherein the via structure does not exceed the first side of the via hole. A first pad is disposed on the first side of the substrate and covering the via hole, wherein the first pad is adjoined to the via structure and electrically connects with the at least one electric device.

The invention provides a method of forming an interconnection structure, comprising providing a substrate having a first side and a second side opposite to the first side, forming a via hole through the substrate, wherein the via hole has a first opening in the first side and a second opening in the second side, forming a first pad covering the first opening, and forming a via structure in the via hole subsequent to forming the first pad, wherein the via structure comprises a conductive material and is adjoined to the first pad.

The invention provides a method for forming an interconnection structure, comprising providing a substrate, forming a via hole through the substrate, and performing a screen printing process on the first side of the substrate to fill a conductive material into the via hole so as to form a via structure in the via hole and a first pad disposed on a first side of the substrate, adjoined to the via structure.

BRIEF DESCRIPTION OF DRAWINGS

The invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein,

FIG. **1**A to FIG. **1**F show intermediate stages of cross sections of a method for forming the interconnect structure of an embodiment of the invention.

FIG. **2** show an intermediate stage of a cross section of a method for forming the interconnect structure of an embodiment of the invention.

FIG. **3**A to FIG. **3**F show intermediate stages of cross sections of a method for forming the interconnect structure of an embodiment of the invention.

DETAILED DESCRIPTION OF INVENTION

It is understood that specific embodiments are provided as examples to teach the broader inventive concept, and one of ordinary skill in the art can easily apply the teaching of the present disclosure to other methods or apparatus. The following discussion is only used to illustrate the invention, not limit the invention.

A method for forming the interconnect structure of an embodiment of the invention is illustrated in accordance with FIG. **1**A to FIG. **1**F. First, referring to FIG. **1**A, a substrate **102** comprising a first side **106** and a second side **108** opposite to the first side **106** is provided. The substrate **102** can be any suitable semiconductor material. For example, the substrate **102** can be Si, SiC, Ge, SiGe, GaAs, InAs, InP or GaN. Next, a buffer layer **104** is formed on the substrate **102**. In an embodiment of the invention, the buffer layer **104** can be a nitride based material to provide good adhesion for the layers thereon and also solve issues of lattice mismatch, but the invention is not limited thereto. The buffer layer **104** can be formed of any suitable material. In an embodiment of the invention, the buffer layer **104** can be aluminum nitride. A first channel layer **110** and a second channel layer **112** are formed on the buffer layer **104**. In an embodiment, the first channel layer **110** can be GaN and the second channel layer **112** can be AlGaN. Thereafter, a first metal layer (not shown) is formed on the first channel layer **110** and is then patterned by lithography and etching to form a source electrode **118** and a drain electrode **120**. In an embodiment of the invention, the first metal layer is a stack of Ti, Al, Ni and/or Au layers. Furthermore, a rapid thermal annealing (RTA) process can be performed to the first metal layer. A second metal layer (not shown) is deposited on the first channel layer **110** and then patterned by lithography and etching to form a gate electrode **116**. Next, a passivation layer **122**, such as silicon nitride and silicon oxide, is formed to protect the device thereunder. The first channel layer **110**, the second channel layer **112**, the gate electrode **116**, the source electrode **118**, and the drain electrode **120** constitute an electric device **114** adjacent to the first side **106** of the substrate **102**. In the embodiment, the electric device **114** is disposed at the first side **106** of the substrate **102**, but the invention is not limited thereto. The electric device **114** can be disposed at the second side **108** of the substrate. **102**. Furthermore, in the embodiment, the electric device **114** is a nitride-based semiconductor device. However, the invention is not limited to a nitride-based semiconductor

device. The invention can be applied to any semiconductor device, such as a silicon based device, III-V group device and/or SOI device.

Next, referring to FIG. **1**B, a photosensitive layer **124** is formed over the substrate **102** Thereafter, referring to FIG. **1**C, the photosensitive layer **124** is patterned by a lithography process and the substrate **102** is further etched using the patterned photosensitive layer **124** as a mask to form a via hole **126** extending through the substrate **102**. In an embodiment, the via hole **126** can be formed with drilling using a laser beam.

Referring to FIG. **1**D, an insulating layer **128** is formed on the sidewall of the via hole **126** for protection. In an embodiment, the insulating layer **128** is silicon oxide and can be formed by thermal oxidation or liquid phase deposition (LPD). Referring to FIGS. **1**E~**1**F, a first pad **130** is formed on the first side **106** of the substrate **102** and covers a first opening **111** of the via hole **126**. The first pad **130** can electrically connect to the electrical device **114** and a second pad **134** formed in subsequent steps, and can comprise a protrusion portion extending into the via hole **126**. In an embodiment, the first pad **130** can comprise silver paste and can be formed by screen printing. Referring to FIG. **1**F, an electroplating process is performed using the first pad **130** as a seed layer to deposit a via structure **132** which fills the via hole **126**. In an embodiment, the via structure **132** and the first pad **130** comprises the same material. In another embodiment, the via structure **132** and the first pad **130** comprises different materials. For example, the via structure **132** can comprise copper. As shown in FIG. **1**F, since the via structure **132** is formed sequentially after forming the first pad **130**, the via structure **132** does not exceed the first opening **111** of the via hole **126** neighboring the first side **106** of the substrate **102**, but can exceed a second opening **113** of the via hole **126** neighboring the second side **108** of the substrate **102**. Next, a second pad **134** is formed on the second side **108** of the substrate **102**. In an embodiment, the second pad **134** can comprise silver paste and can be formed by screen printing. Though not shown in the figure, the invention can further comprise providing another semiconductor substrate which has another electric device thereto, wherein the other electric device electrically connects to the second pad.

In an embodiment of the invention, the electrical device **114** is a high electron mobility transistor (HEMT) and the substrate **102** comprises a conductive substrate. The source electrode **118** is electrically connected to the conductive substrate through the via structure **132**.

A method for forming the interconnect structure of another embodiment of the invention is illustrated in accordance with FIG. **2**. The embodiment of the method for forming the interconnect structure of FIG. **2** is similar to the method of FIGS. **1**E~**1**F and for simplicity its detailed descriptions of similar steps are omitted. The method for forming the interconnect structure of FIG. **2** is different from the method for forming the interconnect structure of FIGS. **1**E~**1**F in that the first pad **202** and the via structure **204** are formed by a single step. In the embodiment, when the through hole **126** depth is not great, for example the depth of the through hole is 20 μm to 50 μm, as shown in FIG. **2**, the screen print for forming the first pad **202** can also fill the through hole **126**, so that formation of the first pad **202** and the via structure **204** can be performed by a single screen printing step.

A method for forming the interconnect structure of yet another embodiment of the invention is illustrated in accordance with FIG. **3**A to FIG. **3**F, The method of the embodiment illustrated in FIG. **3**A to FIG. **3**F differs from the embodiment illustrated in FIG. **1**A to FIG. **1**F by the forming of the pad on the second side of the substrate opposite to the first side with the electric device prior to forming the via structure. First, referring to FIG. **3**A, a substrate **302** comprising a first side **306** and a second side **308** is provided. The substrate **302** can be any suitable semiconductor material. For example, the substrate **302** can be Si, SiC, Ge, SiGe, GaAs, InAs, InP or GaN. Next, a buffer layer **304** is formed on the substrate **302**. In an embodiment of the invention, the buffer layer **304** can be aluminum nitride. A first channel layer **310** and a second channel layer **312** are formed on the buffer layer **304**. In an embodiment, the first channel layer **310** can be GaN and the second channel layer **312** can be A**1**GaN. Thereafter, a first metal layer (not shown) is formed on the first channel layer **310** and is then patterned by lithography and etching to form a source electrode **318** and a drain electrode **320**. In an embodiment of the invention, the first metal layer is a stack of Ti, Al, Ni or Au layers. Furthermore, a rapid thermal annealing (RTA) process can be performed to the first metal layer. A second metal layer (not shown) is deposited and then patterned by lithography and etching to form a gate electrode **316**. An passivation layer **322**, such as silicon nitride and silicon oxide, is formed to protect the semiconductor device thereunder. The first channel layer **310**, the second channel layer **312**, the gate electrode **316**, the source electrode **318**, and the drain electrode **320** constitute an electric device **314** which is adjacent to the first side **306** of the substrate **302**. In the embodiment, the electric device **314** is a nitride-based semiconductor device. However, the invention is not limited to being applied to a nitride-based semiconductor device. The invention can be applied to any semiconductor device, such as a silicon based device, III-V group device and/or SOI device.

Next, referring to FIG. **3**B, a photosensitive layer **324** is formed over the substrate **302** to protect the electric device **314**. Thereafter, referring to FIG. **3**C, the photosensitive layer **324** is patterned by a lithography process and the substrate **302** is further etched using the patterned photosensitive layer **324** as a mask to form a via hole **326** extending through the substrate **302** is formed. In an embodiment, the via hole **326** can be formed by a laser beam.

Referring to FIG. **3**D, an insulating layer **328** is formed on the sidewall of the via hole **326** for protection. In an embodiment, the insulating layer **328** is silicon oxide and can be formed by thermal oxidation or liquid phase deposition (LPD). Referring to FIG. **3**E, a first pad **330** is formed on the second side **308** of the substrate **302** and covers a second opening **311** of the via hole **326**. In an embodiment, the first pad **330** can comprise silver paste and can be formed by screen printing. Referring to FIG. **3**F, an electroplating process is performed using the first pad **330** as a seed layer to form a via structure **332** which fills the via hole **326**. In an embodiment, the via structure **332** and the first pad **330** comprise the same material. In another embodiment, the via structure **332** and the first pad **330** comprise different materials. For example, the via structure **332** can comprise copper. As shown in FIG. **3**F, since the via structure **332** is formed sequentially after forming the first pad **330**, the via structure **332** does not exceed of the second opening **311** neighboring the second side **308** of the substrate **302**, but can exceed a first opening **313** neighboring the first side **306** of the substrate **302**. Next, a second pad **334**, such as silver, is formed on the first side **306** of the substrate **302**.

The method for forming the interconnect structure of embodiments of the invention has advantages as follows. Since the method for forming the interconnect structure of the invention forms the via structure using electroplating with the first pad as a seed layer, no vacuum is required for forming the

interconnect structure. Therefore, the method of the invention can produce semiconductor devices with lower costs.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. It is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. An interconnection structure comprising:

a semiconductor substrate having at least one electric device formed adjacent to a first side of the semiconductor substrate and a via hole formed therethrough, the via hole having a first opening adjacent to the first side of the semiconductor substrate and a second opening adjacent to a second side of the semiconductor substrate opposite to the first side;

a via structure disposed in the via hole without exceeding the second opening; and

a first pad disposed on the second side of the semiconductor substrate and covering the via structure, the first pad comprising a protrusion portion extending into the via hole;

wherein the first pad is adjoined to the via structure and electrically connects with the at least one electric device.

2. The interconnection structure as claimed in claim **1**, wherein the electric device comprises a drain electrode.

3. The interconnection structure as claimed in claim **2**, wherein the via hole passes through the drain electrode.

4. An interconnection structure comprising:

a semiconductor substrate having at least one electric device formed adjacent to a first side of the semiconductor substrate and a via hole formed therethrough, the via hole having a first opening adjacent to the first side of the semiconductor substrate;

a via structure disposed in the via hole without exceeding the first opening;

a first pad disposed on the first side of the semiconductor substrate and covering the via hole; and

a second pad disposed on a second side of the semiconductor substrate opposite to the first side, wherein the via structure comprises a protrusion portion extending into the second pad,

wherein the first pad is adjoined to the via structure and electrically connects with the at least one electric device, and wherein the first pad comprises a protrusion portion extending into the via hole.

5. The interconnection structure as claimed in claim **4**, wherein the electric device comprises a drain electrode.

6. The interconnection structure as claimed in claim **5**, wherein the via hole passes through the drain electrode.

7. An interconnection structure comprising:

a semiconductor substrate having at least one electric device formed adjacent to a first side of the semiconductor substrate and a via hole formed therethrough, the via hole having a first opening adjacent to the first side of the semiconductor substrate;

a via structure disposed in the via hole without exceeding the first opening; and

a first pad disposed on the first side of the semiconductor substrate and covering the via hole;

wherein the first pad is adjoined to the via structure and electrically connects with the at least one electric device.

8. The interconnection structure as claimed in claim **7**, wherein the first pad comprises a protrusion portion extending into the via hole.

9. The interconnection structure as claimed in claim **7**, further comprising a second pad disposed on a second side of the semiconductor substrate, adjoined to the via structure.

10. The interconnection structure as claimed in claim **7**, further comprising an insulating layer disposed on the sidewall of the via hole and surrounding the via structure.

11. The interconnection structure as claimed in claim **7**, wherein the first pad and the via structure are formed of different conductive materials.

12. The interconnection structure as claimed in claim **7**, wherein the first pad and the via structure are formed of the same conductive material.

13. The interconnection structure as claimed in claim **7**, wherein the via structure comprises copper.

14. The interconnection structure as claimed in claim **7**, wherein the first pad comprises silver paste.

15. The interconnection structure as claimed in claim **7**, wherein the via structure comprises a protrusion portion extending into the second pad.

16. The interconnection structure as claimed in claim **7**, wherein semiconductor substrate comprises Si, SiC, Ge, SiGe, GaAs, InAs, InP or GaN.

17. The interconnection structure as claimed in claim **7** further comprising at least one nitride-based semiconductor layer disposed- on the semiconductor substrate.

18. The interconnection structure as claimed in claim **17**, wherein the via hole are formed within the semiconductor substrate and the at least one nitride-based semiconductor layer.

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